PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	Eric J. BERGMAN	EXAMINER:	Z. EL-ARINI
APPLICATION NO.:	10/631,376	ART UNIT:	1746
FILED:	JULY 30, 2003	CONF. NO:	2135

FOR: **METHODS OF THINNING A SILICON WAFER USING HF AND OZONE**

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal was filed on 06/20/2007 with a One Month Extension of Time, responsive to the 02/22/2007 Final Office Action.

[Continued on Next Page.]

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Oct 11, 2007
Date of Electronic Submission

Debbie Gilbert
Signature

Debbie Gilbert
Printed Name

Appeal Brief Under 37 CFR § 1.192(c):

(i) Real Party in Interest.

The real part in interest is Semitool, Inc., a Montana corporation, 655 West Reserve Drive, Kalispell, Montana, 59901.

(ii) Related Appeals and Interferences.

There are no related appeals or interferences.

(iii) Status of Claims.

Claims 20-24, 33-36 and 42-50 are pending and are finally rejected. Claims 1-19, 25-32 and 37-41 are cancelled. The rejection of claims 20-24, 33-36 and 42-50 is appealed.

(iv) Status of Amendments.

No amendments have been filed subsequent to the final rejection.

(v) Summary of Claimed Subject Matter.

The claims describe methods for thinning a silicon wafer. Semiconductor devices are manufactured on silicon wafers. The wafers are typically 200 or 300 millimeters in diameter and about 0.80 millimeters (800 microns) thick. Since the relatively brittle wafers must be handled without breaking while undergoing many (typically hundreds) of process steps, starting with thinner wafers is not practical. On the other hand, the semiconductor end product devices formed on the wafer must ordinarily be much thinner than 0.80 millimeters, to avoid excessive heat build up while

in use, to make dicing the wafer easier, and to reduce the packaging space requirements.

Conventionally wafer thinning methods have various drawbacks. See [0004] - [0008] of the Application, and [0002] – [0005] of Masumoto, U.S. 2004/0214432 A1, discussed at Issue No. 2 below. The claims describe methods for thinning a silicon wafer by initially back grinding or plasma etching. The wafer is then placed into a process chamber. A liquid layer is formed on the wafer surface. The thickness of the liquid layer is controlled. Hydrofluoric acid (HF) is delivered into the chamber and etches the wafer surface (specifically etches away silicon dioxide layer on the surface, exposing fresh silicon). Ozone gas is delivered into the chamber and continually oxidizes the (fresh) silicon surface. This continual etching and oxidizing thins the wafer. See claim 42. Advantages include reduced chemical consumption and waste generation. See [0046].

(vi) Grounds of Rejection to be Reviewed on Appeal.

A. Issue No. 1:

Whether claims 20-24 and 45-49 are unpatentable under 35 U.S.C. 103(a) over EP 782 177 A2 in combination with Park, U.S. Patent No. 5,994,238, or Han et al., U.S. Patent No. 6,740,247.

B. Issue No. 2:

Whether claims 33-36, 42-44 and 50 are unpatentable under 35 U.S.C. 103(a) over EP 782 177 A2 in combination with Park, U.S. Patent No. 5,994,238, or Han et al., U.S. Patent No. 6,740,247, as applied to claims 20-24 and 45-49 above, and further in view of Schaper et al., US 2005/0006738 A1, or Masumoto, U.S. 2004/0214432 A1.

(vii) Argument.

A. Issue No. 1:

The overriding point here is that none of the prior references applied against the claims even arguably suggests controlling the thickness of a liquid layer in a wafer thinning process, and they also do not suggest wafer thinning or the claimed etch rates.

1. The EP 782 177 Reference.

EP 782 177 discloses removing a trace oxide from a wafer using HCl, HF, ozone, or mixtures of them, and water. Paragraph 2 of the 02/22/2007 Final Office Action says (and Applicant agrees) that EP 782 177 makes no suggestion of:

-- wafer thinning;

-- controlling thickness of the liquid layer;

-- etch rates.

Paragraph 5 of the 02/22/2007 Final Office Action on the other hand says that controlling the thickness of the liquid layer is inherent in EP 782 177, because adjusting water flow and spin rate is inherently adjusting the thickness of the liquid layer. Paragraph 5 also says that removing silicon in bulk is not in the claim, and that the claimed etch rates would be adjusted by one skilled in the art to reach optimum results.

Setting the inherency issue aside for the moment, EP 782 177 clearly does not expressly disclose wafer thinning (and indeed there is no contention in the 02/22/2007 Final Office Action that EP 782 177 does disclose wafer thinning). Rather, EP 782 177 discloses etching a trace oxide layer (page 2, lines 41-49) using liquid water, and a gas selected from hydrogen fluoride, hydrogen chloride, ozone and mixtures of them (page 2, lines 55-59).

Relative to the purported inherent disclosure of wafer thinning in EP 782 177, a plain reading of the reference reveals only etching trace oxide layers. See paragraph 5 of the Bergman Declaration (filed under Rule 1.132 on 09/8/2006 and included in the Evidence Appendix). Wafer thinning involves removing material hundreds or thousands of times thicker than an oxide layer—in an unrelated process, conducted for a different purpose, at a different time in the semiconductor device manufacturing process. Hence, EP 782 177 can inherently disclose wafer thinning only through hindsight reasoning.

Turning to EP 782 177 and the controlling the thickness of the liquid layer step as discussed at paragraph 5 of the 02/22/2007 Final Office Action, the only potentially relevant passage in EP 782 177 is the last paragraph on page 3. This paragraph says the rinse step may be controlled by adjusting rinse time, spin rate or water flow rate. The two significant points here are that this description relates to the rinse step (and not to an etching or processing step), and that there is no recognition of any need for, or of achieving, control of the thickness of the liquid layer in EP 782 177 (in a rinse step or in a processing step). Even if the apparatus described in EP 782 177 could be controlled in a way to control the thickness of the liquid layer, there is no suggestion there of doing so.

As for the etch rates of claims 46 and 47, in view of the orders of magnitude differences in the thickness of the material removed, the premise that a person of ordinary skill in the art would adjust the etching rate of EP 782 177 upwardly by hundreds or thousands of times, is simply not reasonable.

2. The Park Reference.

As discussed at paragraph 3 of the Bergman Declaration, Park describes a process for fabricating a semiconductor device using a mixture of ozone gas, anhydrous HF gas, and deionized water vapor. This is a purely vapor process. Col. 3, lines 26-36. There is no mention of use of water, or any liquid, in Park. Indeed, Park avoids use of liquid. Here is what Park says about using a liquid etchant:

> "The conventional wet etchants, such as fluoric acid solution and mixture of fluoric acid, acetic acid and nitric acid, and dry etchants, such as HF gas, CCl_4, CF_4, CHF_3 and etc, alone cannot allow desired etch selection ratio, if generated, between oxide and silicon owing to a difference in the composition of etchant." Col. 2, lines 43-50.

Park criticizes wet etch process as lacking etch selectivity:

> "To etch an oxide film, fluorine compounds are typically used as etchants. For example, an aqueous HF or BOE solution is employed in a wet etch process...
>
> For polysilicon film, a mix aqueous solution of fluoric acid, acetic acid and nitric acid may serve as an etchant in a wet etch process...

These conventional techniques are highly selective between oxide film and silicon film.

* * *

> With such fluorine chemicals, low or similar etch selection ratios are difficult to obtain. Thus, when an oxide or silicon film is needed to a certain extent, a composition suitable to moderately etch them cannot be achieved with such fluorine chemicals." Col. 1, lines 15-32.

Table 1 in Park shows no etching of silicon using an aqueous HF solution. Table 2 in Park shows virtually no etching of silicon with a BOE solution (11 angstroms compared to 300-2000 angstroms using the preferred Park process, Col. 3, lines 38-45). Park accordingly teaches away from a liquid or "wet" process. Since no liquid is used in Park, clearly Park cannot suggest any controlling the thickness of a liquid layer step, as claimed.

As the liquid or wet processes discussed in Park can barely even provide a few angstroms of etching, they certainly cannot suggest any wafer thinning, which requires orders of magnitude greater removal of bulk silicon material. Hence, Park teaches away from wafer thinning using a liquid. Park discusses etching polysilicon or amorphous silicon at an amount of 300-2,000 angstroms. Col. 3, lines 37-45. As set forth at pages 2-3 of the Bergman Declaration, this is not wafer thinning. Moreover, since a wafer 0.80 millimeters thick equates to 8,000,000 angstroms, even removing 2,000 angstroms of material would be insignificant in terms of wafer thinning. In specific terms, claim 45 describes a process where the wafer is thinned to approximately 5-20% of its initial thickness. For a standard wafer about 0.80 millimeters thick, this claimed process removes at least 0.64 millimeters, or 6,400,000 angstroms. This is 3200 times more material removed than in Park.

As described in paragraph 3 of the Bergman Declaration, the etching discussed in Park relates to fabricating a semiconductor device to produce an active electronic circuit. Park does not relate to thinning a wafer, i.e., the substrate on which the semiconductor device is formed, as opposed to the active circuit itself. Even where the substrate is incorporated into the actual device through the formation of transistor regions on the substrate, only the top few hundred angstroms are affected. The remaining much thicker bulk silicon is not part of the device, and is not etched in Park. Moreover, Park is focused on etch selectivity. See the Title, Abstract, Col. 1, lines 8-13, lines 35-40; Col. 2, lines 41-43; Col. 3, lines 27-45. Etch selectivity, i.e., how fast the etchant etches the oxide layer compared to the silicon, is significant only if both are etched simultaneously—which occurs only during device fabrication, and not during wafer thinning. See the Bergman Declaration paragraph spanning pages 2 and 3.

3. The Han et al. Reference.

Han et al., U.S. Patent No. 6,740,247 B1, is applied against the claims for the first time in the 02/22/2007 Final Office Action (at page 3, paragraph 2) as disclosing HF vapor phase cleaning and oxide etching methods. Like Park, Han et al. is a purely vapor phase process. No liquid is used. Indeed, Han et al., again like Park, teaches away from a liquid phase process:

See Han et al. at Col. 1, lines 44-63, which reads in part:

> "...traditional aqueous cleaning processes are less effective or completely ineffective. Thorough drying of rinse solutions from around and in small or high aspect ratio features can be difficult and can result in trapping of contamination at those

> features. Furthermore, new combinations of microelectronic materials and new exotic microelectronic materials can be adversely affected by aqueous cleaning chemicals that historically were considered benign to more conventional materials."

Col. 8, lines 49-56 of Han et al. similarly reads:

> "Such a condensed layer forms when, e.g., for a given water vapor pressure, the selected partial pressure of HF, water, and product are sufficiently high that liquid can exist in contact with the vapor. The etch process in this regime proceeds in a manner that is substantially that of conventional liquid-phase HF etching. Etch product residue and particulate contamination can often occur in this etch regime."

Col. 14, lines 61-67 of Han et al. reiterates avoiding liquid:

> "The multilayer and monolayer HF vapor processes were found for all considerations to be superior over a liquid-phase process."

Clearly, Han et al. teaches away from use of a liquid. Correspondingly, Han et al. cannot suggest controlling a thickness of a liquid layer—since no liquid is used at all.

As for etch rates, Han et al. discloses etching oxide layers 5500 angstroms thick (Examples 2-11 and 16-19). In the remaining examples, oxide layer thickness is not specified. The point here is that in Han et al., the layer removed is 5500 angstroms. A wafer is about 8,000,000 angstroms thick (0.80 mm), i.e., about 1500 times thicker than the oxide layer in Han et al. The examples cited in Han et al. confirm that no thinning is disclosed. Example 2-3 in column 10 results in etching 300 angstroms (0.03 microns) in 3 minutes, equating to a rate of 100 angstroms/minute. The rate in claims 34 and 47 is 50 to 100 times faster. In Han et al., the total amount of material removed is .03 microns. In claims 35, 36, 45, 48 and 50, hundreds of microns of material are removed. Hence, the claimed methods relate to removing thousands of times more material than in Han et al. Han et al. therefore cannot reasonably suggest wafer thinning as claimed. Han et al. also relates only to removing a surface oxide, while the claims relate to thinning the wafer, by removing bulk silicon from the body of the wafer itself.

4. The Combination of EP 782 177 and Park or Han et al.

Initially, combining either Park or Han et al. with EP 782 177 is improper because EP 782 177 is a liquid process, and both Park and Han et al. teach away from using a liquid. Notwithstanding this inherent conflict in the references, the combination does not render the claims obvious -- because even the combination fails to disclose controlling the thickness of the liquid layer. As described above, none of EP 782 177, Park, or Han et al. disclose this step. Moreover, none of these three references reasonably relates to wafer thinning. The etching rates of claims 46 and 47 also cannot be obvious because they are too far above any rates even arguably suggested in these references. The

combination of EP 782 177 with Park or Han et al. accordingly cannot make the claims obvious.

B. Issue No. 2:

Claims 33-36, 42-44 and 50 are rejected over the combination of EP 784 177, Park, or Han, and in view of Schraper or Masumoto. Independent claims 42 and 50 both include the step of back grinding or plasma etching (whereas independent claim 45 discussed above does not). As noted at page 4 of the 02/22/2007 Final Office Action, both Schraper and Masumoto disclose wafer thinning by back grinding or plasma etching. Masumoto also discusses thinning by chemical etching, although back grinding is described as the preferred technique. Neither Schraper or Masumoto disclose thinning a wafer via use of a liquid layer, where the thickness of the liquid layer is controlled. Accordingly, claims 33-36, 42-44 and 50 are patentable for the same reasons as claims 20-24 and 45-49 set forth above.

Applicant accordingly requests that the rejections be reversed.

Dated: October 10, 2007

Respectfully submitted,

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(viii) Claims Appendix.

1-19. (Cancelled)

20. (Previously Presented) The method of claim 45 wherein the HF is delivered into the process chamber in vapor form.

21. (Original) The method of claim 20 wherein the HF vapor is delivered into the process chamber via a carrier gas.

22. (Original) The method of claim 21 wherein the carrier gas comprises ozone.

23. (Previously Presented) The method of claim 20 wherein the oxidized silicon is removed as SiF_4 in vapor form from the process chamber.

24. (Previously Presented) The method of claim 45 wherein the HF is delivered into the process chamber in aqueous form.

25-32. (Cancelled)

33. (Previously Presented) The method of claim 42 wherein the wafer is etched at more than 1000 Angstroms/minute.

34. (Previously Presented) The method of claim 42 wherein the wafer is etched at more than 5000 Angstroms/minute.

35. (Previously Presented) The method of claim 42 wherein the wafer thickness is reduced to 50-100 microns by back-grinding and then by the ozone gas and the HF chemically reacting with the silicon wafer.

36. (Previously Presented) The method of claim 42 wherein the wafer thickness is reduced by at least 400 microns by back-grinding and then by the ozone gas and the HF chemically reacting with the silicon wafer.

37-41. (Cancelled).

42. (Previously Presented) A method of thinning at least one silicon wafer, comprising:

back grinding or plasma etching a surface of the wafer;

placing the wafer into a process chamber;

forming a liquid layer on the surface of the wafer;

controlling a thickness of the liquid layer;

delivering HF into the process chamber, with the HF etching a silicon dioxide layer on the surface of the wafer; and

delivering ozone gas into the process chamber, with the ozone gas continually oxidizing a silicon surface of the wafer exposed by etching the silicon dioxide layer, wherein the HF etches the oxidized silicon surface and thins the wafer.

43. (Previously Presented) The method of claim 42 further comprising spinning the wafer, with the liquid layer substantially uniform and with the spinning helping to control the thickness of the liquid layer .

44. (Previously Presented) The method of claim 42 further comprising forming the liquid layer by spraying liquid onto the wafer.

45. (Previously Presented) A method of thinning at least one silicon wafer, comprising:

placing the wafer into a process chamber;

spinning the wafer;

spraying a liquid including water onto the spinning wafer, with the liquid forming a substantially uniform liquid layer on the wafer;

controlling a thickness of the liquid layer;

providing hydrofluoric acid in the process chamber, with the hydrofluoric acid etching a silicon dioxide layer on a surface of the wafer; and

providing ozone gas in the process chamber, with the ozone gas oxidizing a silicon surface of the wafer exposed by etching the silicon dioxide layer, and with the HF etching the oxidized silicon surface until the wafer is thinned to approximately 5 to 20% of its initial thickness.

46. (Previously Presented) The method of claim 45 with the HF etching the silicon at a rate over 1000 angstroms/minute.

47. (Previously Presented) The method of claim 46 with the HF etching the silicon at a rate of 5000-10000 angstroms/minute.

48. (Previously Presented) The method of claim 45 with the wafer thinned to a thickness of 50-100 microns.

49. (Previously Presented) The method of claim 45 further comprising continuously supplying fresh ozone gas into the process chamber to continually oxidize the exposed silicon surface.

50. (Previously Presented) A method of thinning a silicon wafer, comprising:

back grinding or plasma etching a surface of the wafer;

placing the wafer into a process chamber;

spinning the wafer;

spraying a liquid including water onto the wafer, with the liquid forming a substantially uniform aqueous liquid layer on the surface of the wafer;

controlling a thickness of the aqueous liquid layer;

providing hydrofluoric acid in the process chamber, with the hydrofluoric acid removing a silicon dioxide layer on a surface of the wafer and exposing a silicon surface on the wafer;

supplying ozone gas into the process chamber, with the ozone gas continually oxidizing the exposed silicon surface of the wafer until the wafer is thinned to 50-100 microns.

(ix) Evidence Appendix.

1. Declaration of Eric J. Bergman Under 37 C.F.R. 1.132.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	ERIC J. BERGMAN	EXAMINER:	Z. EL-ARINI
APPLICATION NO.:	10/631,376	ART UNIT:	1746
FILED:	JULY 30, 2003	CONF. NO:	2135
FOR:	**METHODS OF THINNING A SILICON WAFER USING HF AND OZONE**		

DECLARATION OF ERIC J. BERGMAN UNDER 37 C.F.R. 1.132

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Sir:

I, Eric J. Bergman, declare:

1. I am the inventor of the methods claimed in Application No. 10/631,376, entitled Methods of Thinning a Silicon Wafer Using HF and Ozone. I have over fifteen years of research and development experience in semiconductor processing. Much of my research and development work has been on ozone-based processing of semiconductor wafers. I am an author of multiple articles in this field. I am employed as a Process Engineer at Semitool, Inc., the Assignee of this Application. I am a named inventor on over 40 U.S. patents and patent applications. Several of these patents and applications relate to processing with ozone.

2. I have reviewed the prior art references cited in the 6/13/06 Final Office Action in connection with the claims in the present application and make the following observations:

3. **The Park Patent** - The Field of the Invention section in Park states the invention relates to "a method for fabricating a semiconductor device and, more particularly, to use of a mixture phase of ozone gas, anhydrous HF gas and deionized water to control the etch selection ratio between oxide film and polysilicon film." Park is very specific that his process is used for the fabrication of a semiconductor device, which reflects a clear intent that his process is used for producing an active electronic circuit.

In other words, Park is not directed to thinning a wafer or a semiconductor substrate (the substrate being the platform on which the semiconductor device is formed, as opposed to the actual active circuit itself). Indeed, Park discloses a method for fabricating a semiconductor device, not for etching a semiconductor wafer. Even where the substrate is incorporated into the actual device through the formation of transistor regions in the substrate, this only incorporates the top few-hundred angstroms of the substrate into the device. The remaining material is not part of the device, and, in fact, is generally considered detrimental to the device, which is why as much of this material as possible is typically removed prior to packaging.

Wafer thinning occurs at only two times in the life of a wafer: (1) during the manufacture of the wafer before any device structure is formed on the wafer - this is done to bring the substrate material into specification for thickness and surface

finish; and (2) after all device fabrication has been completed. The wafer is thinned in order to make dicing of the wafer easier and to optimize packaging of the finished device. The wafer is most commonly single-crystal silicon. It may be GaAs or some other III-V compound, but it is never polysilicon. Persons skilled in semiconductor device manufacturing recognize that "etching" does not imply "thinning" of the substrate. A polysilicon etch implies that thinning of the single-crystal silicon substrate is not an objective and is not performed.

In Park, the objective is to etch a thermal oxide- and polysilicon-exposed wafer. Thus, Park deals with wafers having both exposed oxide and exposed polysilicon. Park describes having a low etch selectivity between a silicon oxide film and polysilicon, which is important only if both films are simultaneously exposed. Both of these films would be present only during device fabrication, which indicates that Park is performing a pattern etch, not a wafer-thinning operation. The possibility that a minimal amount of wafer substrate material might be consumed during the etching process is not an objective, but a potential side-effect. However, Park, by stating that his process is to be used to etch polysilicon and oxide, specifically implies that the single-crystal substrate (i.e., the wafer) would not be etched to a significant degree, since the single-crystal silicon substrate would not have polysilicon and silicon oxide simultaneously exposed.

Park envisions his process to be used for forming the active region of the device. He intends to simultaneously etch polysilicon and silicon oxide at a low selectivity in order to retain the physical dimensions of the structure. In my 21 years of experience in the semiconductor industry, I have never encountered a polysilicon

substrate for semiconductor device fabrication. In device fabrication, I have etched silicon, polysilicon, silicon dioxide, silicon nitride, aluminum, tungsten, cobalt, nickel, platinum, gold, numerous silicides, and various other exotic films, such as hafnium oxides. All of these were etch processes. None of these are done with the intent of thinning the wafer, because thinning a wafer is not consistent with device fabrication as in Park.

4. **The EP '177 Patent** - The EP '177 patent teaches removing an oxide film from a semiconductor wafer. EP '177 lists ozone in passing as one of several different gases that may be used. However, the EP '177 process is performed using HF gas. The top of page 4 of EP '177 discusses preventing undesirable oxidation of the etched silicon surface, and avoiding use of water having dissolved ozone to avoid oxidation. Logically, ozone, which is an even stronger oxidizer, should also be avoided, based on this content of EP '177. On the other hand, the process in the claims of my application include use of ozone.

5. **Combination of Park and EP '177**

The EP '177 patent discloses etching a silicon dioxide film (not the wafer substrate) to minimize oxygen on the wafer surface. Park discloses a low selectivity etch of silicon oxide and polysilicon by using HF gas, ozone gas, and water vapor. If these two patents are combined, the result is a method for removing silicon dioxide and polysilicon using anhydrous HF and ozone with water vapor, followed by a rinse which may use anhydrous HF and ozone. There is still nothing there in the combination to reasonably instruct thinning a wafer.

There is also nothing in the combination relevant to the etch rates described in claims in my application. The etch rate taught by Park is simply a number. Park shows four graphs and two tables. None of these contain any silicon or polysilicon etch rate data. The only silicon or polysilicon data in these graphs and tables are from conventional aqueous HF or BOE processes. The data that Park provides in the body of his patent, indicating a polysilicon etch rate of up to 50A/sec, cannot be applied to single-crystal silicon, which generally etches very differently from polysilicon. There is simply no way to combine the teachings of Park with the teachings of EP '177 to obtain the process of my application, particularly since neither

. I hereby declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 under Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: Sept. 8, 2006

Eric J. Bergman

(x) Related Proceedings Appendix.

None.